

Attorney's Docket No. 003424.P018
Express Mail No.: EL651844325US

UNITED STATES PATENT APPLICATION

FOR

**APPARATUSES AND METHODS FOR FORMING ELECTRONIC
ASSEMBLIES**

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0992406-061701
"9042E660"

APPARATUSES AND METHODS FOR FORMING ELECTRONIC ASSEMBLIES

BACKGROUND INFORMATION

Field of the Invention

[0001] The present invention relates generally to the manufacturing of electronic assemblies, and more particularly to the manufacture of display devices.

Description of Related Art

[0002] Electronic assemblies such as display devices are known in the art. Display devices include a variety of displays such as field emission displays (FEDs), plasma display devices, and other suitable display devices. Each of these display devices are described below.

[0003] FEDs are generally used for television images, oscilloscope radar displays, computer displays, and other like applications. **Figure 1** illustrates a cross-sectional view of a FED known in the art. FEDs are comprised of anode 2 and cathode 8. Anode 2 comprises multiple layers of material. These multiple layers include a face layer 6, a vacuum layer 18, a conductive layer 20, and a luminescent layer 22. As noted in United States Patent No. 5,818,165, the face layer 6 of the anode 2 may be comprised of flexible material.

[0004] Face layer 6 has a top and bottom surface. The bottom surface of face layer 6 is parallel to cathode 8. Face layer 6 must be comprised of material that allows the face layer 6 to have sufficient strength to maintain a vacuum.

Vacuum layer 18 is introduced onto the bottom side of face layer 6. Vacuum layer 18 also has a top and bottom side. The top side of vacuum layer 18 is adjacent to face layer 6. Vacuum layer 18 may be comprised of a flexible material such as silicon dioxide (SiO_2), silicon nitride (Si_3N_4), or silicon carbide (SiC).

[0005] Conductive layer 20 is formed onto the bottom surface of the vacuum layer 18. Conductive layer 20 may be approximately 1500 Å thick and comprised of indium tin oxide or other conductive material. Luminescent layer 22 is formed onto the bottom surface of conductive layer 20. The

luminescent material may be comprised of phosphorous (P) or other luminescent material.

[0006] Cathode 8 is parallel to the anode 2. Cathode 8 is also comprised of multiple layers. Cathode 8 has a backing layer 10, a plurality of conductors 12, a resistive layer 24, insulating layer 28, and a gate electrode layer 26. Backing layer 10 may be comprised of a flexible metal layer such as aluminum laminated to a flexible insulating layer 28.

[0007] Conductors 12 are located on the interior of the backing layer 10. Conductors 12 includes conductive material such as niobium (Nb), aluminum (Al), or other like elements. Conductors 12, approximately 2,000 Å thick, may be parallel strips that intersect at right angles.

[0008] Resistive layer 24 includes resistive material such as silicon (Si) or silicon compounds, is formed on conductors 12 and backing layer 10. The resistive layer may be 10,000 Å – 12,000 Å thick. Insulating layer 28 is deposited on top of the resistive layer 24 and may be comprised of silicon dioxide (SiO₂). Insulating layer 28 may be 1.0-1.2 µm thick. Gate electrode layer 26, formed on top of the insulating layer 28, may be comprised of Nb and have a thickness of 2,000 Å. Gate electrode layer 26 may be formed through physical deposition (e.g. sputtering, evaporation, etc.) onto the insulating layer, chemical vapor deposition, or the like.

[0009] A gap of approximately 200 µm exists between the anode 2 and the cathode 8. This gap may be created by inserting a nonconductive layer of approximately the thickness of the gap. A flexible frit 30 may include a material such as glass fibers bound together with epoxy materials is formed between anode 2 and cathode 8.

[0010] Spacer 921 supports the display against the atmospheric pressure and allows the display area to grow without increasing the thickness of either the anode or the cathode. To seal anode 2 and cathode 8, the device described above undergoes an annealing process. The annealing process operates at a temperature that causes the epoxy material to melt away. Flexible layer 16 is wrapped over the insulating layer 28 creating a vacuum seal with flexible frit 30. The vacuum or negative pressure in the gap is maintained by flexible frit 30, flexible layer 16, and vacuum layer 18 that is disposed completely around the periphery of the display 1.

[0011] A picture is created on a FED having an anode which has a transparent conductive material coating on a transparent display screen. When the electrons collide with the screen, the point of collision forms all or part of a picture element (*e.g.*, pixel) of a displayed image. The higher the rate of collision of electrons with the anode 2, the greater the brightness of the pixel.

[0012] FEDs have either active or passive matrix panels. Active and passive matrix panels may be transmissive. Transmissive displays include polysilicon thin-film transistor (TFT) displays and high-resolution polysilicon displays.

[0013] **Figure 2** is a schematic diagram of a portion of a passive matrix FED that includes rows 36A-36C of extraction grids and columns 34A-34C of emitters 913. The emitters 913 emit electrons when an appropriate voltage is applied to a row 36A-36C and a column 34A-34C. The shift register 301 receives a horizontal synchronization signal that activates buffers 32A-32C. Buffers 32A-32C provide a grid voltage from a grid voltage generator 31 to rows 36A-36C of the extraction grid. Emitter drive currents are generated by circuits 38A-38C. The emitter drive currents are proportional to the luminance signals to the columns 34A-34C.

[0014] **Figure 3** is a schematic diagram of a portion of an active matrix FED. An emitter drive circuit 44 is created by a pair of negative-channel metal oxide semiconductor (NMOS) transistors 40 and 42 together with a resistor that is serially coupled between the emitters 46. FED 50 has one continuous extraction grid 48 that is generally active on a continuous basis when the FED 50 is in use. Emitters 46 are activated by an enable signal that is applied to the gate of transistor 40 in which the transistor 40 acts as a closed switch.

[0015] **Figure 4** illustrates a conventional emitter 14. Generally, emitters 14 are cone-shaped where the top of the cone is thinner than the bottom of the cone shape. Emitters 14 may be comprised of conductive material such as molybdenum (Mo) or other suitable material. When an emitter 14 is excited, electrons are emitted from the tip of the emitter which occurs when an enable signal is applied to the gate of a transistor.

[0016] **Figure 5** illustrates a cross-sectional view of a FED of the prior art. FEDs have a substrate that has recessed regions for emitters. Spacers are used to separate the anode from the cathode. Phosphor dots are parallel to the substrate. Black matrix is interspersed between the spacers and the phosphor dots.

[0017] **Figure 6** illustrates a cross-sectional view of a FED of the prior art. Anode 2 is parallel to cathode 903. Gates are located between emitters. A frit seal 909 is connected to anode 2 and cathode 903. External column driver chip is coupled to the substrate used for cathode 903. Red, green, and blue phosphor dots 70 are parallel to the emitters.

[0018] Fabrication of plasma displays is well known in the art and is generally described in U. S. Patent No. 5,844,373. Plasma displays are typically used for advertisements, portable computers, or any other type of displays that require a large screen size.

[0019] As shown in **Figure 7**, a plasma display typically comprises a cell such as a liquid crystal cell 901, a plasma cell 4, and a dielectric layer 905 interposed between them. Dielectric layer 905 is thin for driving the liquid crystal cell 901, and a thin plate glass with a thickness of about 50 μm surrounds the dielectric layer 905. The liquid crystal cell 901 includes a substrate 8A that is comprised of glass and electrode 12 that are in the main inner surface of the substrate 8A. Substrate 8A is coupled to the dielectric layer 905. Gap 911 is created using spacers 24. Liquid crystal material fills gap 106.

[0020] Plasma cell 4 includes a substrate 22 that is typically comprised of glass and a plurality of electrodes (also referred to as rods) 18 are formed in a stripe pattern on the main surface of the substrate 22. Gap 911 exists between the dielectric layer 905 and substrate 22. Gap 911 is created between dielectric layer 905 and substrate 22 by barrier ribs 907 and frit seals 909 as illustrated in **Figure 9**. Barrier ribs 907 are usually 100 to 300 μm in height and 100 μm width. Although barrier ribs 907 are shown on top plasma electrodes, barrier ribs 907 may be spaced apart and not be contacted with the plasma electrodes or barrier ribs 907 may be formed apart from the plasma substrate glass such as on the dielectric layer 905. Frit seals 909 are typically comprised of a low melting glass. An ionizable gas such as helium, neon, argon, xenon or a mixture thereof is sealed in the space created by barrier ribs 907 and frit seal 909. Barrier ribs 907, formed on each of the plasma electrodes by a means such as screen printing process, create space for the plasma cell. Plasma cell 4 is divided by the barrier ribs 907 into stripe portions that constitute electric discharge channels.

[0021] Plasma displays create an image based upon the principle that an electrical discharge in an inert gas causes luminescence. A surface discharge

display panel has fluorescent material that emit light when excited by ultraviolet light. As voltage is applied sequentially to scanning electrodes, lines on the display screen are selected one by one. In conjunction with the selection of lines, three data electrodes intersect the line that is selected. Because the three data electrodes correspond to primary colors of light such as red, green, and blue, a picture element (*e.g.* a pixel) is formed on the display screen. A picture element is created when the discharge channel and the signal electrode D intersect.

[0022] Three voltages are generally required to form and maintain a display of a plasma display panel: (1) a voltage V_a of approximately 50 volts is typically applied to data electrodes; (2) voltage V_s of approximately 180 volts is required for maintaining discharge is applied to the sustaining electrodes; and (3) an entire surface discharge sustaining voltage V_d of approximately 330 volts.

[0023] Plasma electrodes 12 act alternately as an anode and a cathode to generate a plasma discharge. The discharge is substantially defined by barrier ribs 907.

[0024] As shown in **Figure 8**, display electrodes and data electrodes are disposed on the front plate and the base plate. These display electrodes are comprised of discharge scanning electrodes. As mentioned above, while voltage is applied to the discharge sustaining electrodes, lines on the display screen are selected one by one. Three data electrodes correspond to three primary colors such as red (R), green (G), and blue (B). Three points (R, G, B) where the data electrodes intersect the line that is selected by discharge sustaining electrodes and composes a pixel element (*e.g.* pixel) on the display screen.

[0025] Voltage of approximately 50 volts is required for starting a discharge and is applied to the data electrodes. Maintaining the discharge requires a voltage of approximately 180 volts to be applied to both the discharge sustaining and scanning electrodes. Approximately 330 volts is applied to the discharge sustaining electrodes to start a discharge over the entire surface of the display panel (hereinafter referred to as entire-surface discharge). The display panel, therefore, requires a data selection voltage of approximately 50 volts, an entire-surface-discharge-starting voltage of approximately 330 volts, and a discharge-sustaining voltage of approximately 330 volts.

[0026] The display is created when voltage is applied to the sustaining electrodes in the entire surface discharge and a ground is applied sequentially to the discharge scanning electrodes, lines are scanned and selected one after another. The data electrodes are driven according to the display data to be displayed on the line, the display cells on the selected line discharge and display the display data. Reading of the display data for each display cell from the I/O buffers drives the data electrodes. The display cell discharges or does not discharge depending upon whether voltage or ground is applied to the data electrodes.

[0027] As shown in **Figure 9**, a plasma display has a liquid crystal cell coupled to a dielectric sheet. The liquid crystal cell has a uniformly thin sheet of glass that is approximately 50 μm . The dielectric sheet is also coupled to a plasma cell. The plasma cell is surrounded by an uniformly thin sheet of glass that is approximately 50 μm .

[0028] These plates are parallel to each other and are typically comprised of glass. The two glass plates of a plasma display are separated by spacers and sealed and evacuated. One of the glass plates (*e.g.*, face plate) has a screen that has light-emitting material on it or under it, such as plasma, a phosphor, or a color filter or other medium.

[0029] **Figure 10** illustrates a rod 14A and a circuit element 18 on the top surface of a cylindrical rod 14A. These rods may take a variety of shapes but they are generally elongated and rectangular in shape.

[0030] Figure 11 illustrates a portion of an array in an active matrix display backplane for a plasma display. Plasma displays may have an alternate type of active matrix liquid crystal array. The control line rows in this device are coupled to gate electrodes along a row and the control line columns are coupled to data drivers which supply pixel voltages which are applied to the pixel electrodes. A column line 34 is connected to a source electrode of field effect transistor (FET). Another column line is coupled to a source electrode of FET. A row line 32 is coupled to the gates of both FETs 36 and 37. The drain of FET 36 is coupled through capacitor 923 to a transparent pixel electrode along the row 32 formed by FETs 36 and 37, and the drain of FET 37 is coupled through a capacitor to another pixel electrode along the row. In one typical example, the backplane may be formed by depositing rods using an FSA technique into a rigid substrate (e.g., glass). Each rod contains a FET and a

capacitor and is interconnected to other rods by column and row conductors that are deposited onto the rigid substrate; and, the capacitor is coupled to a pixel electrode by another conductor that is deposited onto the rigid substrate. The active medium (*e.g.*, plasma) is placed between the base and face plates which will optically change the active medium's properties in response to the combined voltages or currents produced by the pixel electrodes. The active medium at a given pixel electrode 42 will appear as a square or dot in the overall checkerboard type matrix of the display. The actual size of the FETs and the pixel electrodes are not now drawn to scale, but are shown schematically for the purposes of illustration. The interconnect (*e.g.*, rods) between the rows and columns is comprised of flexible and conductive material. For example, the interconnect could be made of aluminum, copper, gold or other conductive materials.

[0031] A circuit using a complimentary metal oxide semiconductor (CMOS) technology (not shown) and a diffused metal on silicon (DMOS) transistor are also used in a plasma display. CMOS is used for illumination and pulse control and generally relates to linking a PMOS (a semiconductor doped with a p-type dopant) transistor device with an NMOS (a semiconductor doped with n-type dopant) device. CMOS is used outside of the array. DMOS is used for high power plasma displays.

[0032] There are several disadvantages inherent to display devices such as FEDs. For example, the FED described in United States Patent No. 5,818,165 discloses a FED in which the plurality of emitters and gates are created on one layer of the cathode of the FED. This is inefficient because a portion of the emitters will be inoperable. Additionally, FEDs are typically manufactured by using deterministic methods to place driver chips and spacers onto one of the layers of the cathode. This reduces productivity because it is more efficient to use a method in which premanufactured objects are quickly placed onto a layer.

[0033] Another disadvantage to existing FEDs is that they are typically manufactured in a batch operation. Batch operations inherently involve a certain amount of down-time in production. This increases aggregate production time to fabricate display panels. Moreover, flat-panel displays are generally fabricated on substrates which are not continuous in length. This

also decreases productivity since the assembly of the flat-panel displays is interrupted until another panel is available to assemble the flat-panel display.

[0034] There are also several disadvantages associated with conventional plasma displays. For example, plasma displays are also manufactured using deterministic methods with regard to placing rods onto one of the glass plates such as the base plate. This reduces productivity because it is more efficient to use a method in which objects are quickly placed onto the rigid substrate, such as through fluidic self assembly. Another disadvantage to plasma displays is that they are also typically manufactured in a batch operation. It is therefore desirable to have a method of manufacturing display devices such as FEDs and plasma displays that overcome the disadvantages associated with conventional display device.

SUMMARY OF THE INVENTION

[0035] One aspect of the present invention provides various apparatuses and methods for creating a FED using the process of fluidic self-assembly (FSA) to assemble objects (*e.g.*, blocks having emitters and gates, spacers, and driver chips) into a substrate.

[0036] Another aspect of the invention relates to creating blocks having a plurality of emitters and gates. While creating emitters and gates are known in the art, segregating blocks having emitters and gates from a substrate is new. This feature allows the blocks to be tested prior to being assembled onto a receiving substrate. The blocks are separated from the substrate by using an etchant such as hydrofluoric acid.

[0037] Another aspect of the invention relates to an operation that occurs after the FSA has been performed. To verify that the FSA process results in complete placement of objects, a "pick and place" process is utilized. "Pick and place" allows the objects to be placed into empty recessed regions on the receiving substrate which were missed during the FSA process. The substrate is first checked for empty recessed regions by using an electronic eye that views the substrate for empty recessed regions. Once an empty recessed region is detected, a robot is used to "pick and place" an object into an empty recessed region of the substrate.

[0038] Another embodiment of the invention relates to fluidic self assembly (FSA) that is used to place rods with all of the necessary logic such as control logic that is in each rod onto at least one substrate. These rods form a portion of the backplane that is used in an active matrix plasma display. FSA may also be used to place barrier ribs and spacers onto a substrate.

[0039] While an array of components (*e.g.* display components) for an assembly have been described as examples of the invention, an array of other assemblies such as x-ray detectors, radar detectors, micro-electro-mechanical structural elements (MEMS) or, generally, an assembly of sensors or actuators or an assembly of circuit elements also may be produced using the claimed invention. Thus, for example, flexible antennas, other sensors, detectors, or an array of circuit elements may be fabricated using one of the embodiments of the inventions. Other aspects and methods of the present invention as well as apparatuses formed using these methods are described further below in conjunction with the following figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0040] The present invention is illustrated by way of example. The invention is not limited to the figures of the accompanying drawings in which like references indicate similar elements. Additionally, the drawings are not drawn to scale.

[0041] **Figure 1** illustrates a cross-sectional view of a FED in the prior art.

[0042] **Figure 2** illustrates a passive matrix for a FED in the prior art.

[0043] **Figure 3** illustrates an active matrix for an FED in the prior art.

[0044] **Figure 4** illustrates an emitter in the prior art.

[0045] **Figure 5** illustrates a cross-sectional side view of a FED in the prior art.

[0046] **Figure 6** illustrates a planar side view of a FED in the prior art.

[0047] **Figure 7** illustrates a configuration of a plasma display panel of the prior art.

[0048] **Figure 8** illustrates a configuration of electrodes of a plasma display panel of the prior art.

[0049] **Figure 9** illustrates a planar side view of a plasma display of the prior art.

[0050] **Figure 10** illustrates a rod of the prior art.

[0051] **Figure 11** illustrates an array in an active matrix of a plasma display of the prior art.

[0052] **Figures 12A-12O** show an assembly of blocks having emitters and gates, spacers, and driver chips on a substrate.

[0053] **Figures 13A-13E** show a double-template transfer of objects to a substrate in accordance with one embodiment of the invention.

[0054] **Figures 14A-14E** show another embodiment of a double-template transfer in accordance with one embodiment of the invention.

[0055] **Figure 15** illustrates a flow chart of the method of assembling a display by depositing blocks having emitters and spacers onto the substrate in accordance with one embodiment of the invention.

[0056] **Figure 16** illustrates a flowchart of the method of manufacturing multiple displays along a substrate in accordance with one embodiment of the invention.

[0057] **Figure 17** illustrates a top view of a substrate with multiple display components fabricated thereon in accordance with one embodiment of the invention.

[0058] **Figure 18** illustrates a top view of a display component which has an active matrix display backplane attached thereto in accordance with one embodiment of the invention.

[0059] **Figure 19** illustrates a top view of substrate attached to a display backplane in accordance with one embodiment of the invention.

[0060] **Figure 20A** illustrates a flow chart of a method of fabricating a display device wherein a substrate and a display tape undergo processing and are subsequently coupled in accordance with one embodiment of the invention.

[0061] **Figure 20B** illustrates a method of fabricating a display device wherein a substrate and a display tape undergo processing and are subsequently coupled in accordance with one embodiment of the invention.

[0062] **Figure 21** illustrates a flow chart of a method of the picking and placing objects onto a substrate after the FSA process has been applied to the substrate in accordance with one embodiment of the invention.

[0063] **Figure 22** illustrates a flow chart which relates to the FSA process and the coupling of the display material to the substrate in accordance with one embodiment of the invention.

[0064] **Figure 23** illustrates a top view of a continuous substrate wherein displays of different sizes are created in accordance with one embodiment of the invention.

[0065] **Figure 24** illustrates a top view of a continuous substrate wherein displays of similar size are created in accordance with one embodiment of the invention.

[0066] **Figure 25** illustrates a planar side view of the recessed regions in the substrate in accordance with one embodiment of the invention.

[0067] **Figure 26A** illustrates a planar side view of a substrate in accordance with one embodiment of the invention.

[0068] **Figure 26B** illustrates openings or receptor regions created and emitters deposited onto the substrate in accordance with one embodiment of the invention.

[0069] **Figure 26C** illustrates deposition of planarization material and openings being created in the substrate in accordance with one embodiment of the invention.

[0070] **Figure 26D** illustrates another material placed over a portion of the blocks in accordance with one embodiment of the invention.

[0071] **Figures 27A-27G** illustrate recessed regions created in a substrate and FSA being used to assemble structures onto the substrate.

[0072] **Figure 28** illustrates a flow chart of the method of assembling a rigid display by depositing rods onto the rigid substrate.

[0073] **Figure 29** illustrates a flowchart of the method of manufacturing multiple displays along a rigid substrate.

[0074] **Figures 30A through 30F** illustrate one embodiment of double template transfer of rods.

DETAILED DESCRIPTION

[0075] The present invention relates to apparatuses and methods for forming displays and other electronic assemblies. The following description and drawings are illustrative of the invention and are not to be construed as limiting the invention.

[0076] One embodiment of the invention relates to using FSA to form a display such as a FED display. Incorporated by reference is United States Patent No.

5,545,291 explaining how to assemble objects onto a substrate using FSA. The FSA with a plurality of objects is deposited onto the substrate wherein the objects fall into recessed regions found in the substrate. One embodiment has the objects (*e.g.*, blocks having emitters and gates, spacers, and driver chips) being transferred at one time.

[0077] The various objects may be placed into recessed regions of a substrate by using FSA first for the largest objects. After the largest objects are placed in the largest recessed regions of the substrate using a first slurry, a second slurry containing the next smallest size objects is dispensed onto the substrate. In an alternative embodiment, all of the various sized objects could be placed into a slurry and dispensed at one time over a substrate. After the objects have been dispensed onto the substrate, the substrate is then advanced to a further point in the process in which an interconnect layer is deposited onto the substrate. While the substrate is advanced, a display tape is advanced to a point where the substrate becomes coupled to the display tape.

[0078] In another embodiment of the invention, various rods, each containing a functional component, may be fabricated on one substrate and then separated from that substrate and assembled onto a separate rigid substrate through FSA.

[0079] Another embodiment of the invention relates to the FSA process wherein, after the objects are deposited on the substrate, they fall into recessed regions found in the substrate. After a certain time period, the substrate is checked for any existing empty recessed regions. Finding empty recessed regions is accomplished by using an electronic eye attached to a machine which is able to view the surface of the substrate. A robot or a person is used to place an object into an empty recessed region.

[0080] In the following description, numerous specific details such as specific materials, processing parameters, processing steps, *etc.*, are set forth in order to provide a thorough understanding of the invention. One skilled in the art will recognize that these details need not be specifically adhered to in order to practice the claimed invention. In other instances, well known processing steps, materials, *etc.*, are not set forth in order not to obscure the invention.

[0081] Field Emission Displays (FEDs) are described followed by Plasma Displays. A substrate refers to either a rigid substrate or a flexible substrate. A rigid substrate may comprise glass, soda lime glass, silicon, plastic, quartz, or other suitable material. Flexible substrates may be comprised of PES,

polyethylene terephthalate, polycarbonate, polybutylene terephthalate, PPS, polypropylene, polyester, aramid, PAI, polyimide, aromatic polyimides, polyetherimide, metallic materials, ABS, PVC, or other suitable material.

[0082] **Figures 12A-12O** illustrate an assembly of blocks and spacers onto a substrate. Blocks having emitters and gates which are created by using photolithography and by applying a mask and etch material. Then, an etching material is applied to the substrate comprised of glass. An assembly of the type described herein may be used in credit cards, watches, computers, televisions, radar, computer displays, a variety of like displays, or electronic devices.

[0083] **Figure 12A** illustrates a first substrate 52 in accordance with one embodiment of the invention. First substrate 52 is comprised of a rigid material such as glass. First substrate 52 is coupled with an insulating layer 54 deposited thereon. Insulating layer 54 may be comprised of insulating materials such as silicon dioxide (SiO_2) and may have a thickness of 1.0-1.2 μm . Dielectric material 53 is sandwiched between the insulating layer 54 and first substrate 52. **Figure 12B** illustrates a gate electrode layer 56 deposited on the surface of the insulating layer 54. Gate electrode layer 56 may be formed by sputtering, evaporation onto the insulating layer, chemical vapor deposition, or other suitable operation. Gate electrode layer 56 is comprised of conductive materials such as Nb and may have a thickness up to 2,000 Å. **Figure 12C** illustrates a masking material such as conventional photoresist deposited on gate electrode layer 56. Mask 58 is used for designation of areas which are not to be etched. This masking material may form a layer that has a thickness of approximately 2 microns. **Figure 12D** illustrates the same device as in **Figure 12C**, but the masking material is shown to mark designated layers on the gate electrode layer 56. **Figure 12E** illustrates a layer of etchant 60 deposited on top of the masking layer as shown in **Figure 12D**. The etchant used depends on the metalization used. The mask and etch of the device in **Figure 12E** creates cavities in the insulating and gate electrode layers. **Figure 12F** illustrates a lift-off layer of material, such as nickel, deposited by an electron beam deposition process, or other suitable method, over the gate electrode layer 56 to form a sacrificial lift-off layer. **Figure 12G** illustrates a sacrificial layer 59 comprised of some type of photoresist on top of the device shown in **Figure 12F**. **Figure 12H** illustrates a conductive tip material 62 (e.g., molybdenum (Mo)) deposited

within each cavity by using a beam of electrons which are normal to the apertures created in the insulating and gate electrode layers. Thereafter, a material such as a variety of acids is used to lift-off the blocks having the emitters and gates from the substrate. **Figure 12I** illustrates a material such as hydrofluoric acid that separates a block with the emitters and gates which creates the device in **Figure 12J**. **Figure 12J** illustrates a block that holds a plurality of emitters and gates. Although the block shows three emitters and three gates, there may be a greater or lesser amount of emitters and gates created on the blocks. By fabricating a plurality of blocks with emitters and gates thereon, these microelements may be tested to ensure that they are operable before the objects are placed on the substrate (or a flexible layer). **Figure 12K** illustrates a substrate with recessed regions created within the substrate. There are shaped recessed regions of various sizes for the purpose of receiving a variety of objects. **Figure 12L** illustrates blocks having emitters and gates that have slid into the recessed regions of the substrate. These blocks were placed into their respective positions through the FSA process. **Figure 12M** illustrates a spacer that has been placed into a recessed region which is slightly larger in diameter than the spacer itself. The spacer also was placed in this position through the FSA process (or through the "pick and place" method if the FSA process does not place the spacer into a recessed region for the spacer). **Figure 12N** illustrates the same device as in **Figure 12M** except that a driver chip has been placed into a recessed region which has a diameter which is slightly larger than the driver chip itself. The driver chip also was placed in this position through the FSA process. **Figure 12O** illustrates a first substrate and a second substrate coupled together. The first substrate forms a portion of the cathode and the second substrate forms a portion of the anode.

[0084] **Figures 13A-13E** illustrate another embodiment of the invention involving template transfer of a plurality of objects. **Figure 13A** illustrates recessed regions that are a variety of shapes. These various shapes allow for the various sized objects to be placed into their respective sized shaped recessed regions. The recessed regions are slightly larger than the objects that they are to receive. **Figure 13B** illustrates a first template in which the FSA process was used to place a plurality of objects into their respective regions by use of a vacuum pump. The plurality of objects may be held in place by a variety of methods such as through a vacuum being applied to the first

template. If the vacuum is applied during the FSA process, the plurality of objects may be attracted to their respective regions. Another method involves using release tape on the first template. Release tape has a Teflon (e.g., PFA) backing that is made by Norton Performance Plastics. The release tape holds the plurality of objects in place. After the objects are seated in the first template, the release tape is placed on top of the plurality of objects. **Figure 13C** illustrates the first template as in **Figure 13B** in which a second template having at least one side that has recessed regions faces the first template with a plurality of objects protruding therefrom. **Figure 13D** illustrates a template being coupled to the receiving substrate wherein the various sized objects are inserted into the receiving substrate. **Figure 13E** illustrates that the templates are detached from one another. A plurality of objects are released from the first template by a variety of methods. For example, if a vacuum is used to hold the blocks in place, the vacuum is broken allowing the plurality of objects to be released from the first template. If release tape is used to hold the plurality of objects to the first template, the first template is heated allowing the release tape to release the plurality of objects. Heat may be applied by a variety of methods. For example, convection may be used to transfer heat to the first template. The material may be placed between the first template and the heat source. The materials used should be able to conduct heat.

[0085] Figures 14A-14E illustrate another embodiment of the double-template transfer in which individual types of objects are transferred to a receiving substrate. While these figures show the end result of each type of object transferred to recessed regions made to receive that particular object, the steps used to transfer a type of object is based upon the double-template transfer method as illustrated in U.S. Patent Application Serial No. 09/270,159 entitled "*Methods and Apparatus for Fabricating A Multiple Modular Assembly.*" **Figure 14A** illustrates a template that has various shaped recessed regions. **Figure 14B** illustrates the transfer of a first shaped object to the template. For example, a block having emitters and gates is shown to be transferred to the first template by FSA. If FSA is unable to transfer all of the blocks to the first template, the "pick and place" method may be used to place the block onto the first template. The double-template transfer, as described above, may then be used to transfer the plurality of blocks to the first template. **Figure 14C** illustrates that a spacer has been transferred to the first template. **Figure 14D** illustrates the plurality of

objects have been transferred completely using the methods described herein such as FSA or “pick and phase.” **Figure 14E** illustrates a second template coupled to the first template. **Figure 14F** illustrates that the plurality of objects have been released from the first template and are attached to the second template. The plurality of objects are released from the first template for example by breaking the vacuum. If release tape is used to hold the blocks in place, a plurality of objects are released by applying heat to the tape causing the plurality of objects to be released.

[0086] While **Figures 14A-14F** illustrate the single transfer of blocks having emitters and gates, driver chips, and spacers, these objects could undergo double-template transfer in a different order. For example, the driver chip could be placed first into recessed regions rather than using FSA to place the blocks first onto the first template. Similarly, any combination of two or more objects may be placed onto the first template by FSA using the double-template method described above.

[0087] **Figure 15** illustrates one method of assembling a display along the length of a substrate 80 in accordance with an embodiment of the invention. Objects are assembled into the openings of the substrate at operation 80. Utilizing an FSA process, blocks having a plurality of emitters and gates are deposited in a slurry. The blocks then go into the recessed regions of the substrate by sliding into recessed regions of the substrate. A plurality of spacers is then deposited onto the substrate. The spacers then slide into recessed regions of the substrate. Driver chips also may be deposited onto the substrate. Planarization of the assembly of objects into a substrate is the next operation 82. A variety of methods may be used to planarize the various objects. For example, planarization may take place by depositing a material which may be used to flatten the plurality of objects or may be subjected to conventional chemical-mechanical polishing. Then, the electrical coupling of the plurality of blocks takes place at 84 by opening holes in the planarization layer and depositing metalization material or other conductive materials into the holes and beyond the holes to form an interconnect (*e.g.*, a row or column interconnect) between the blocks. The display is made to conform the object's shape at operation 88. A display generation substrate (*e.g.*, a phosphor layer) is coupled to the active matrix backplane at operation 89.

[0088] **Figure 16** illustrates a method of manufacturing multiple displays along a substrate. Multiple display components are created on a substrate at operation 200. The substrate is advanced to a second region of the substrate at operation 202. A new display component is created on the substrate in a different region of the substrate at operation 204 by advancing the substrate through a web processing apparatus at operation 206. Separation of the display panel from the production line occurs at the end of the process at operation 210.

[0089] **Figure 17** illustrates a substrate with multiple display components. Substrate 220 has display component 222 and display component 224 attached thereto. Substrate 220 has three lengths: a first length 226, a second length 228, and a third length 230. Display components 222 and 224 are active matrix display devices.

[0090] **Figure 18** illustrates a first substrate 50 attached to a passive display backplane 52 that may be used to form a display device.

[0091] **Figure 19** illustrates a display component 925 that has an active matrix display backplane 22A attached thereto that may be used to form a display device.

[0092] **Figure 20A** illustrates a method of fabricating a display device in which a substrate and a display tape undergo processing and are subsequently coupled. The substrate is advanced along a process line at operation at operation 500. A first slurry containing a plurality of blocks in which each block has a plurality of emitters and gates is dispensed onto the substrate at operation 502. The first slurry also may contain a variety of additional objects such as driver chips and spacers. This is the preferred embodiment. Other embodiments entail each individual object separately dispensed onto the substrate and each object slides into recessed regions that are slightly longer than the objects that they are set to receive. In these embodiments, each type of object has its own container before it is dispensed and each type of object is separately recycled.

[0093] A second slurry containing a plurality of blocks, spacers, and driver chips is again dispensed onto the substrate in order to fill each recessed region that was not filled by dispensing the first slurry. Excess slurry is collected in a container and is recycled. The blocks, spacers, and driver chips slide into the

recessed regions that they are sized to fit. Adhesives are then deposited onto the substrate at operation 504.

[0094] **Figure 20B** illustrates the overall process of fabricating a display device in which a first substrate 120 and a second substrate 160 undergo processing and are subsequently coupled. The first substrate is advanced along a first process line and advances through a first set of support members 122. A first slurry 124 containing a plurality of blocks having emitters thereon, spacers, and driver chips is dispensed onto the first substrate. A second slurry 126 containing a plurality of objects (*e.g.* blocks, spacers, and driver chips) is again dispensed onto the first substrate. Excess slurry is collected in a container 128 and is recycled. The blocks fall into recessed regions in the substrate. First substrate 120 is advanced through a second set of support members 130. At operation 132, the first substrate undergoes planarization as illustrated in **Figures 26A-26D**. The first substrate is then advanced to point 134. At operation 175, a second substrate is coupled to the first substrate. While the process may follow the operation outlined below, it will be appreciated that it is also possible that one portion of the display will be singulated prior to the second substrate being secured to the first substrate.

[0095] **Figure 21** relates to a method of picking and placing of objects onto a substrate after the FSA process has been applied to the substrate. A slurry containing a plurality of objects is dispensed onto the substrate at operation 90. Then the objects fall into recessed regions in the substrate. The excess slurry is collected and recycled at operation 91. The substrate is checked for empty recessed regions at operation 92. This checking is performed by an electronic eye which views the substrate. Objects are robotically placed into empty regions found in substrate at operation 94. At operation 98, the second substrate is coupled to the first substrate.

[0096] **Figure 22** relates to the FSA process and the coupling of the display material with the substrate. At operation 431, it is determined whether the recessed regions are equivalent in size. A slurry containing a plurality of blocks having emitters and gates thereon is deposited onto the substrate at 410. If the recessed regions are of equivalent size, operation 450 is then followed. A single slurry is deposited onto a substrate at operation 450. (Excess slurry is caught and recycled at operation 460.) If the recessed regions are not of equivalent size (*e.g.*, the blocks have varying numbers of emitters), operation

410 is followed. A first slurry with a first plurality of objects is deposited onto the substrate at operation 410. Excess slurry is caught and recycled at operation 415. Once this operation is performed, a second slurry with a second plurality of objects is placed onto the substrate at operation 420. Excess second slurry is recycled into a second container at operation 425.

[0097] **Figure 23** illustrates a continuous substrate in which two displays are created. Display device 52 is larger than display device 50. This shows that multiple displays of different sizes can be created on the substrate through an in-line process. Alternatively, **Figure 24** illustrates displays 926 and 927 of similar size.

[0098] In addition to multiple displays being able to be made different sizes, the substrate itself may have different sized recessed regions. This allows the substrate to receive various sized blocks or devices. **Figure 25** illustrates a cross-sectional view of the recessed regions in the substrate. Recessed region 931 is smaller than recessed region 937.

[0099] **Figures 26A-26C** illustrate generally the process of planarization material being added onto the substrate. **Figure 26A** illustrates a planar side view of a substrate 190. **Figure 26B** illustrates openings or receptor regions 192 created and blocks having emitters and gates deposited into the substrate. **Figure 26C** illustrates deposition of planarization material 194 and openings being created into the substrate. **Figure 26D** illustrates a second material 198 placed over a portion of the blocks with emitter and gates thereon.

[00100] The formation of plasma displays by implementing techniques of the invention is described below relative to **Figures 27-31**. **Figures 27A-27G** illustrate the assembly of rods onto a substrate. **Figure 27A** illustrates a first substrate 662. The first substrate 662 is comprised of glass but other rigid material may be used. **Figure 27B** illustrates a planar side view of recessed regions or apertures 669 created in first substrate 662. First substrate 662 has a plurality of recessed regions that are sized and shaped to receive rods 614. In this particular embodiment, a recessed region has a diameter slightly greater than the diameter of the object that it is established to receive. For example, rods 614 are sized and shaped slightly smaller than the recessed regions that are set to receive them. **Figure 27C** illustrates recessed regions for spacers 668 and recessed regions 679 for barrier ribs 666 are created in the substrate and are slightly larger than the diameters of the objects that they are set to receive.

These recessed regions may be created in a variety of methods such as that which is described in co-pending U.S. Patent Application Serial No. 09/270,165 entitled "*Apparatuses and Methods for Forming Assemblies*" (Docket No. 003424.P016).

[00101] **Figure 27D** illustrate a cross-sectional view of rods 614 deposited into their respective recessed regions 669. **Figure 27E** illustrates spacer 668 placed into recessed region 675. **Figure 27F** illustrates barrier rib 665 in recessed region 685.

[00102] In one particular embodiment as shown in **Figure 27G**, the first substrate 662 has a coating of conductive material such as aluminum. Gettering material 676 may be deposited onto first substrate 662. Gettering material 676 is used for the purpose of collecting gaseous contaminants within a display. These materials may include zirconium/vanadium iron alloy, zirconium metal, or materials having aluminum or titanium. These materials may be found in powdered form or may be liquefied and used to adhere with the first substrate 662. The gettering materials may have a low melting point alloy such as indium alloy. Gettering material also may be applied by electrophoretic deposition, screen printing, or other methods described below. First substrate 662 is connected to a direct current (DC) voltage source (not shown). This DC voltage source applies a suitable voltage up to at least 400 volts.

[00103] The first substrate 662 is conductive in order to bleed off impinging charge. In one particular embodiment, the first substrate 662 includes a glass substrate that has a coating of conductive material such as aluminum. Gettering material 676 for collecting gaseous contaminants within the display may also be deposited onto the glass substrate.

[00104] Spacers 668 are dispensed onto the rigid substrate. Spacers 668 separate the face plate and the base plate. Rods 614 are deposited onto the rigid substrate and are part of the active matrix display backplane. Rods 614 drive a picture element (not shown).

[00105] **Figure 28** illustrates one method of assembling a rigid display along the length of a rigid substrate in accordance with an embodiment of the invention. Objects (*e.g.*, rods) are assembled into the openings of the rigid substrate of operation 670. Utilizing an FSA process, a plurality of rods are deposited in a slurry that go into the recessed regions of the rigid substrate. A

plurality of barrier ribs and spacers 668 are then deposited onto the rigid substrate.

[00106] Planarization of the assembly of objects into substrate is the next operation 672. Planarization takes place by a variety of methods such as depositing a material that may be spun to flatten certain objects that were dispensed onto the substrate or may be subjected to conventional chemical-mechanical polishing. Then, the electrical coupling of the plurality of rods 614 takes place at 674 by opening holes in the planarization layer and depositing metalization material or other conductive materials into the holes and beyond the holes to form an interconnect (*e.g.*, a row or column interconnect). The display is made to conform the object's shape 678. A display generation substrate (*e.g.*, plasma layer) is coupled to the active matrix backplane 680.

[00107] **Figure 29** illustrates a method of manufacturing multiple displays along a substrate. Multiple display components are created on a substrate at operation 700. The substrate is advanced to a second region on the substrate at operation 702. A new display component is created on the rigid substrate in a different region of the substrate at operation 704 by advancing the substrate through a web processing of apparatus at operation 706 and coupling a display material to the substrate at operation 708. Separation of the display panel occurs at the end of the process 710.

[00108] **Figures 30A** through **30E** show planar side views as to how the transfer of rods with circuit elements thereon are transferred to substrates that are used to form displays or other assemblies. **Figure 30A** illustrates a planar side view of a template (donor substrate) 855. **Figure 30B** illustrates recessed regions in template 855. These recessed regions may be made by a variety of conventional methods and another method described in co-pending U.S. Patent Application Serial No. 09/270,157 entitled "*Methods for Transferring Elements From A Template to a Substrate*" (Docket No. 003424.P009). **Figure 30C** illustrates a first plurality of objects dispensed onto template 855. In this embodiment, rods 660, barrier ribs 662, and spacers 664 are dispensed onto template 855. It will be appreciated that these objects may be dispensed in several operations such as dispensing each type of object in one operation or a variety of objects may be dispensed onto template 855 in an operation. If the objects do not fill all of the recessed regions, a second plurality of objects may be dispensed onto template 855. Template 855 may be comprised of rigid

material such as metal including steel, stainless steel, molybdenum, aluminum, invar, beryllium, copper, brass, and glasses such as quartz, soda lime, borosilicate or plastics such as polyimide, polyamide, ABS, PVC, acrylic, polycarbonate, nylon, and ryton. These templates are manufactured by a variety of methods such as injection molding or by using a press that makes impressions into a template base comprised of the materials listed above.

Figure 30C illustrates a planar side view of a template 855 in which rods 660 are seated in recessed regions. The rods may be kept in place by a variety of methods. In one case, the rods may be deposited by FSA onto the template and then secured by a release tape which is placed over the rods and the top surface of the template. Additionally, electrostatic forces or vacuum may be used to hold the rods in place.

[00109] **Figure 30D** illustrates a planar side view of a template 855 holding the rods. In this embodiment, the template 855 is inverted over a receiving substrate 853. However, the receiving substrate 853 may be placed over the template and pressed against the template 855. A variety of other positions may be used when transferring rods to a receiving substrate 853 but the important factor is that template 855 with the plurality of rods must contact at least one side of the receiving substrate 853. Contact of just the plurality of rods 660, barrier ribs 662, and spacers 664 may be sufficient to perform the transfer. The receiving substrate 853 may have recessed regions or holes or the rods in the template 855 and may create recessed regions or holes in the receiving substrate when the template contacts the receiving substrate 853. In an alternative embodiment, the rods are released from the template by using a material such as release tape. The release tape is heated causing the rods to be released from the template. The heat is applied through conventional sources such as convection. Another embodiment of the invention allows the rods to be released from the template by pressure. Pressure may be applied mechanically such as through a press. **Figure 30D** illustrates a planar side view of the template 855 contacting the receiving flexible substrate 853. **Figure 30E** illustrates the rods being transferred to the receiving substrate. **Figure 30F** illustrates another embodiment of the end result of a planar side view of the template 855 after it is removed from the receiving rigid substrate 853 and the rods have been transferred. Here, the rods are inverted, showing that the rods

may be transferred in which a portion of the rods is transferred to the receiving substrate 857.

[00110] While an array of components (*e.g.*, display components) for an assembly have been described as examples of the invention, an array of other assemblies such as x-ray detectors, radar detectors, micro-electro-mechanical structural elements (MEMS) or, generally, an assembly of sensors or actuators or an assembly of circuit elements also may be produced using the claimed invention. Thus, for example, flexible antennas, other sensors, detectors, or an array of circuit elements may be fabricated using one of the embodiments of the inventions. Other aspects and methods of the present invention as well as apparatuses formed using these methods are described further below in conjunction with the following figures.

[00111] Listed below are related U.S. patent applications that describe various improvements to the methods and devices of the invention described herein. These patent applications and a U.S. Patent are incorporated by reference.

[00112] Co-pending U.S. Patent Application Serial No. 09/270,146 entitled "*Apparatuses And Methods For Forming Assemblies*" (Docket No. 003424.P008), filed by Jeffrey J. Jacobsen, Glenn Wilhelm Gengel, and Gordon S. W. Craig and assigned to the same Assignee as the present invention, describes an electronic modular assembly. This co-pending application is hereby incorporated herein by reference.

[00113] Co-pending U.S. Patent Application Serial No. 09/270,157 entitled "*Methods For Transferring Elements From A Template To A Substrate*" (Docket No. 003424.P009), filed by Jeffrey J. Jacobsen, Mark A. Hadley, and John Stephen Smith and assigned to the same Assignee of the present invention, describes an FSA on a template with transfer to another substrate. This co-pending application is hereby incorporated herein by reference.

[00114] Co-pending U.S. Patent Application Serial No. 09/270,159 entitled "*Methods and Apparatuses For Fabricating A Multiple Module Assembly*" (Docket No. 003424.P010), filed by Jeffrey J. Jacobsen, Glenn Wilhelm Gengel, and Gordon S. W. Craig and assigned to the same Assignee as the present invention, describes an electronic modular assembly. This co-pending application is hereby incorporated herein by reference.

[00115] Co-pending U.S. Patent Application Serial No. 09/270,147 entitled "*Apparatuses And Methods Used In Forming Electronic Assemblies*" (Docket No. 003424.P011), filed by Jeffrey J. Jacobsen, Glenn Wilhelm Gengel, and John Stephen Smith and assigned to the same Assignee as the present invention, describes a method of molding substances. This co-pending application is hereby incorporated herein by reference.

[00116] Co-pending U.S. Patent Application Serial No. 09/268,755 entitled "*Web Process Interconnect In Electronic Assemblies*" (Docket No. 003424.P012), filed by Jeffrey J. Jacobsen, Glenn Wilhelm Gengel, Mark A. Hadley, Gordon S. W. Craig, and John Stephen Smith and assigned to the same Assignee as the present invention, describes a method of creating various interconnects on a web tape. This co-pending application is hereby incorporated herein by reference.

[00117] Co-pending U.S. Patent Application Serial No. 09/270,165 entitled "*Apparatuses And Methods For Forming Assemblies*" (Docket No. 003424.P016), filed by Jeffrey J. Jacobsen and assigned to the same Assignee as the present invention, describes a method of rolling objects into their recessed regions. This co-pending application is hereby incorporated herein by reference.

[00118] United States Patent No. 5,545,291 entitled "*Method For Fabricating Self-Assembling Microstructures,*" filed by John S. Smith and Hsi-Jen J. Yeh, issued August 13, 1996, is hereby incorporated herein by reference.

[00119] In the foregoing detailed description, the invention is described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.